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Z6104

4096 x 1 Bit Static RAM

Zilog

Product Specification

JANUARY 1978

Preliminary

Features

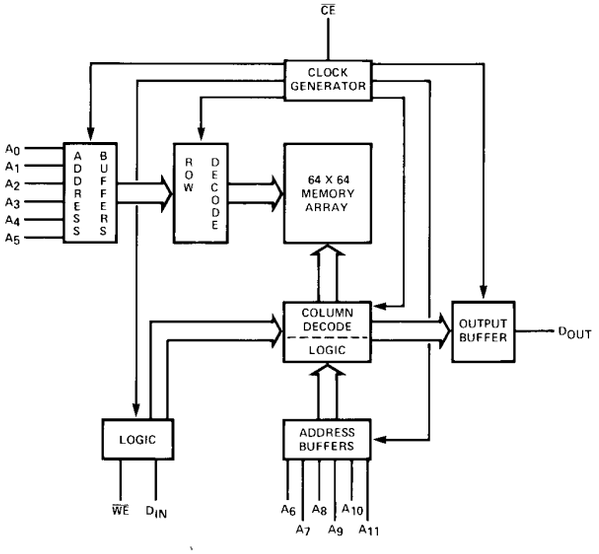
- 4096 X 1 organization
- Static data storage circuitry (no refresh required)
- Single phase chip enable clock generator circuitry
- Separate data in and data output pins
- Access/Cycle times: / Operating power*

Access/Cycle times:	Operating power*	
100/160 ns	320 mW	Z6104-1
150/240 ns	320 mW	Z6104-2
200/320 ns	320 mW	Z6104-3
250/380 ns	165 mW	Z6104-4
300/440 ns	165 mW	Z6104-5
350/510 ns	165 mW	Z6104-6

*T_A = 70°C

- All input pins are TTL voltage level compatible
- Single +5V power supply (±10%)
- Industry standard 18 pin DIP
- Advanced depletion load N channel silicon gate technology

Functional Block Diagram



Description

The Zilog Z6104 is a 4096 x 1 static RAM, fabricated using n-channel depletion load silicon gate technology. Polysilicon load resistors are used in the 64 x 64 memory array, resulting in a very small die size.

CHIP ENABLE is used as the clock input to the RAM. The HIGH-to-LOW edge of $\overline{CE}$ initiates data movement within the chip, resulting in the appearance of valid data at the D_{OUT} pin. When $\overline{CE}$ is HIGH, the device is in the precharge mode and the chip's standby power is reduced from its operating power. Since the Z6104 is static, $\overline{CE}$ can be stopped at any time in the precharge mode without the loss of data.

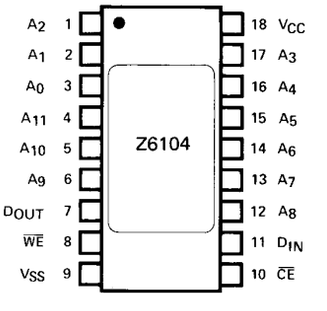
The twelve address pins select a cell within the memory array. These inputs are strobed into the RAM address buffers with the $\overline{CE}$ HIGH-to-LOW edge.

WRITE ENABLE controls the circuit's read/write function. When the RAM is activated by $\overline{CE}$, a LOW voltage on $\overline{WE}$ writes the data presented at the D_{IN} pin to the selected memory cell.

Virtually all MOS circuits draw less current at elevated temperature than at cold temperature. For this reason, the Z6104 has two power limits. The cold limit is necessary for system power supply design while the hot limit is useful for thermal air movement calculations.

D_{OUT} is capable of driving two TTL loads or up to eight low-power Schottky TTL loads to standard TTL voltage output levels. All inputs are specified to standard TTL input voltage limits.

Pin Connections



Pin Names

$A_0 - A_{11}$	ADDRESS INPUTS
$\overline{CE}$	CHIP ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{SS}	GROUND
V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE

1403

004524

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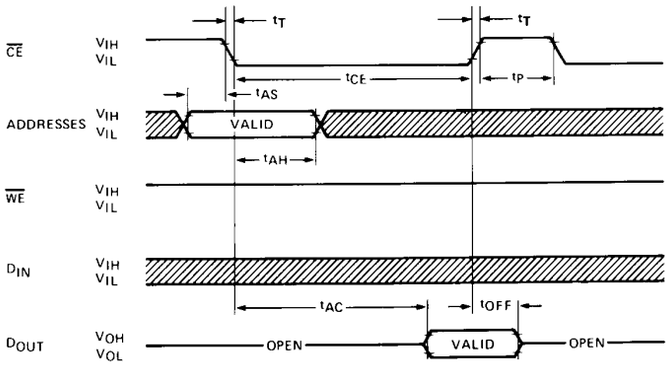
Operation and Timing Waveforms

Read Cycle

The twelve address pins have their information latched on $\overline{CE}$'s low going edge.

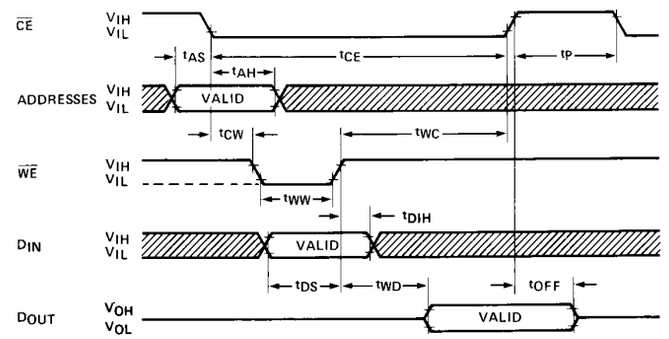
With $\overline{WE}$ HIGH, $\overline{CE}$'s HIGH-to-LOW transition will cause the information stored at the location specified by the address inputs to appear at D_{OUT}. D_{OUT} starts in the high impedance mode (inactive) and goes to a low impedance mode (active) after the access time. When $\overline{CE}$ returns HIGH, D_{OUT} goes inactive.



Write Cycle

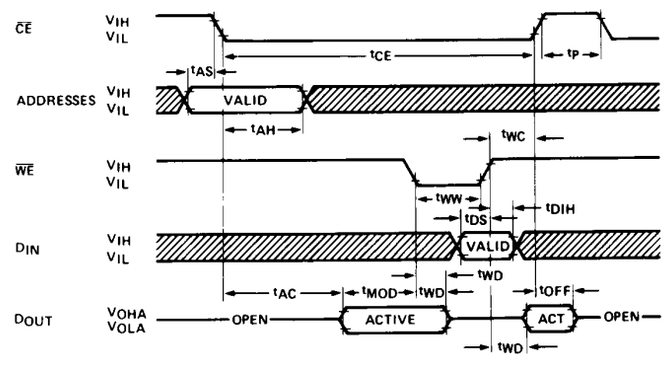
Data to be written into the chip from the Data Input pin is loaded into the selected location on the later occurring edge of $\overline{CE}$ or $\overline{WE}$. The data must remain stable for the required set-up and hold times about either $\overline{WE}$ or $\overline{CE}$ edge, whichever occurs first. When writing, D_{OUT} is inactive, but when $\overline{WE}$ returns HIGH, D_{OUT} goes active indicating the logic state of the addressed cell until $\overline{CE}$ returns HIGH.

It is possible to use the 6104 in an "early write" mode. $\overline{WE}$ can be taken LOW at or before the beginning of the cycle, but $\overline{WE}$ cannot go HIGH until $(t_{CW} + t_{WW})$ after $\overline{CE}$'s LOW-going edge.

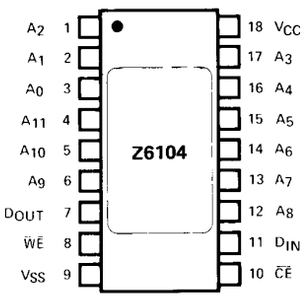


Read/Modify/Write Cycle

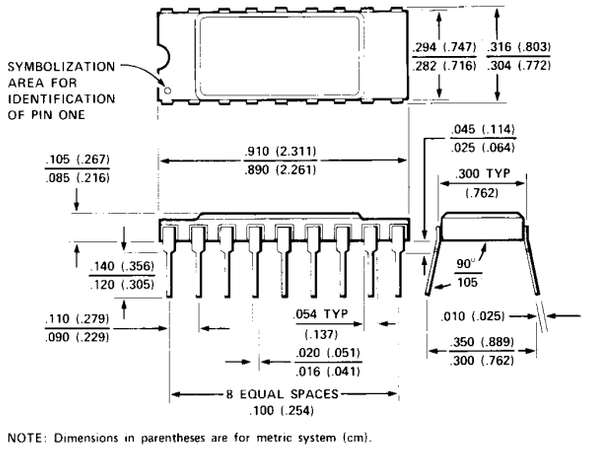
This is an extension of the Read and Write cycles. Data is read after an access time and in the same cycle is modified with a Write operation. For this cycle D_{OUT} starts inactive, and goes active after the write. At the end of the cycle, signified by $\overline{CE}$'s positive edge, D_{OUT} becomes inactive.



Package Configuration



Package Outline



NOTE: Dimensions in parentheses are for metric system (cm).

Absolute Maximum Ratings*

Voltage on any pin relative to V_{SS} . . . . . –0.3V to +7.0V
Storage Temperature (Ambient) . . . . . –65°C to +150°C
Power Dissipation . . . . . 1.5 Watts
Temperature under bias. . . . . Specified operating range

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended D.C. Operating Conditions

($0°C < T_A < +70°C$)

SYMBOL	PARAMETER	Z6104		UNIT
		MIN	MAX	
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IH}	Logic 1 Voltage (All Inputs)	2.0	V_{CC}	V
V_{IL}	Logic 0 Voltage (All Inputs)	–0.3	0.8	V

D.C. Electrical Characteristics

($0°C < T_A < +70°C$) (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	$T_A = 0°C$				$T_A = 70°C$				UNIT
		Z6104-1,2,3		Z6104-4,5,6		Z6104-1,2,3		Z6104-4,5,6		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
I_{CC1}	Average V_{CC} Power Supply Current (1)		80		40		58		30	mA
I_{CC2}	Standby V_{CC} Power Supply Current (2)		60		30		44		23	mA
$I_{I(L)}$	Input Leakage Current (any input)		10		10		10		10	μA
$I_{O(L)}$	Output Leakage Current (2, 3)	-10	10	-10	10	-10	10	-10	10	μA
V_{OH}	Output Logic 1 Voltage (I_{OUT} = -200 μA)	2.4		2.4		2.4		2.4		V
V_{OL}	Output Logic 0 Voltage (I_{OUT} = 3.2 mA)		0.4		0.4		0.4		0.4	V

NOTES:
1. A function of $\overline{CE}$ duty cycle. Measured with duty cycle of $t_{CE}/(t_{CE} + t_p)$
2. $\overline{CE}$ @ V_{IH}
3. $0.4V \leq V_{OUT} \leq 5.5V$

Capacitance

($0°C < T_A < +70°C$) (V_{CC} = +5.0V ± 10%)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{IC}	Input Capacitance ($\overline{CE}$, $\overline{WE}$)		5	pF
C_I	Input Capacitance ($A_0 - A_{11}$, D_{IN})		5	pF
C_O	Output Capacitance		10	pF

A.C. Electrical Characteristics

($0°C < T_A < +70°C$) ($V_{CC} = +5.0V \pm 10\%$)

SYMBOL	PARAMETER	Z6104-1		Z6104-2		Z6104-3		Z6104-4		Z6104-5		Z6104-6		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_C	Read or Write Cycle Time (3)	160		240		320		380		440		510		ns
t_{AC}	Random Access (1)		100		150		200		250		300		350	ns
t_{CE}	Chip Enable Pulse Width	100		150		200		250		300		350		ns
t_P	Chip Enable Precharge Time	40		60		80		100		120		140		ns
t_{AH}	Address Hold Time	40		50		80		100		120		140		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		ns
t_{OFF}	Output Buffer Turn-off Delay (2)		40		40		50		60		80		100	ns
t_{CW}	Chip Enable to Write Enable	40		50		60		80		100		120		ns
t_{DIH}	Data Input Hold Time	30		40		40		40		40		40		ns
t_{WW}	Write Enable Pulse Width	40		40		50		60		80		100		ns
t_{MOD}	Modify Time		100		100		100		100		100		100	μs
t_{WD}	Write Enable to Data Out (2)	0	40	0	50	0	60	0	80	0	100	0	120	ns
t_{DS}	Data Input Set-up Time	50		60		70		80		100		120		ns
t_{WC}	Write Enable to Chip Enable	0		0		0		0		0		0		ns
t_T	Transition Time		50		50		50		50		50		50	ns

NOTES:
1. Output loaded with 100pF and 2 TTL loads. Output levels are $V_{OH} = 2.0V$ and $V_{OL} = 0.8V$
2. Output waveform is dependent on output load. D_{OUT} is guaranteed to be OFF within t_{OFF}.
3. $t_C = t_{CE} + t_P + 2 \cdot t_T$

Further Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±10% 0°C to 70°C

Example:
Z6104CS (Ceramic – Standard range)

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